UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,172	03/11/2004	Reiji Hattori	04171/LH	1045

1933 7590 05/15/2007

FRISHAUF, HOLTZ, GOODMAN & CHICK, PC
220 Fifth Avenue
16TH Floor
NEW YORK, NY 10001-7708

EXAMINER	
TRAN, HENRY N	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
05/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,172	HATTORI, REIJI	
	Examiner	Art Unit	
	Henry N. Tran	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) *13,14,16-39,42-44,50-59 and 62-76* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,15,40,41,45-49,60 and 61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of the Species I, Fig. 1, claims 1-12, 15, 40, 41, 45-49, 60 and 61, in the reply filed on 2/28/07 is acknowledged.

2. Claims 13, 14, 16-39, 42-44, 50-59, and 62-76 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 2/28/07.

Information Disclosure Statement

3. The examiner has considered the documents listed in forms PTO/SB/08A/B submitted with the Information Disclosure Statements (IDSs) received 3/11/04, 3/12/07, and 4/17/07 (see the attached forms PTOPTO/SB/08A/B).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 40 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakuragi (U.S. Patent No. 6,222,357).

Regarding claim 1, Sakuragi, Fig. 1, teaches a current drive apparatus which operates a plurality of loads (light emitting elements: D1, D2, ...) by applying a current thereto, the current drive apparatus comprising: a plurality of output terminals (2, 3, ...) to which the loads are respectively connected; a single current generation circuit (6) (a current output type D/A converter) which outputs an operating current having a predetermined current value ("the predetermined reference current"); and a plurality of current storage circuits comprising hold capacitors C1, C2, ...), which are respectively connected to the output terminals, sequentially fetch and hold the operating current, and simultaneously output a drive current based on the operating current to the output terminals, see col. 3, line 65 to col. 4, lines 27, and col. 4, line 58 to col. 5, line 29.

Regarding claims 40 and 41, Sakuragi further teaches a drive method of a current drive apparatus which operates a plurality of loads connected to a plurality of output terminals by applying to a current thereto, the drive method comprising the step of: generating an operating current having a predetermined current value ("the predetermined reference current") by a single current generation circuit (6) and outputting it to a plurality of current storage circuits; sequentially fetching and holding the operating current into the respective current storage circuits; and simultaneously outputting a drive current based on the operating current held in the current storage circuit to the respective output terminals; wherein the step of holding the operating-current in the respective current storage circuits and the step of outputting the drive current to the respective output terminals are executed in parallel (the switching devices, e.g., S1 and S2, are turned on, or controlled "at the same time"), see, Fig. 1, and col. 5, lines 3-23.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-12, 15, 45-49, 60, and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuragi (U.S. Patent No. 6,222,357) in view of Ozawa (U.S. Patent No. 6,765,560).

Regarding claim 2, Sakuragi teaches generally all as discussed above except expressly teaches that the operating current has a current value according to an input signal. Ozawa does teach a current drive apparatus which operates a plurality of loads (light emitting elements 11) by applying a current thereto, the current drive apparatus comprising current generation circuit (23) (a current output type D/A converter) which outputs an operating current, which is an analog image signal (Sa), having a predetermined current value according to an input signal, which is digital image signal (Sg), see Fig. 5, col. 6, lines 27-32, and col. 7, line 18 to col. 8, line 38. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the current output type D/A converter as taught by Ozawa for the Sakuragi D/A converter because this would accurately and efficiently supply the current value of the analog image signal for displaying the desired images, see Ozawa, col. 8, lines 33-38, and lines 55-58. Claim 2 is dependent upon the base claim 1; and is therefore rejected on the same reasons set forth in claim 1, and by the reasons discussed above.

Regarding claims 3-6, Sakuragi in view of Ozawa (hereinafter referred to as "Sakuragi-Ozawa") teaches all the claimed limitations. For example, Sakuragi further teaches: (i) an output current generation circuit, which comprises a pair of switching devices: M1 and M2, which generates and outputs an output current having a predetermined current ratio relative to the control current, see col. 4, lines 12-23; wherein the current value of the control current is set larger than a current value of the output current, see col. 5, lines 31-32; and the output current generation circuit comprises a current mirror circuit (provided by a pair of switching devices: M1 and M2, M3 and M4, etc ...) having the predetermined current ratio, see col. 6, lines 9-15.

Ozawa further teaches: (i) a control current generation circuit which generates a control current (Sa) according to the input signal (Sg); wherein the input signal is a digital signal having a plurality of bits, the control current generation circuit comprises a plurality of bit current generation circuits which generate a plurality of bit currents that current values have weightings corresponding to respective bits of the digital signal, and any of the respective bit currents are selected in accordance with a bit value of the input signal, and the control current is generated by adding the selected bit currents, see the references above. Claims 3-6 are dependent upon the claim 2; and are therefore rejected on the same reasons set forth in claim 2, and by the reasons noted above.

Regarding claims 7-12, 15, 45-49, 60, and 61, Sakuragi-Ozawa teaches all the claimed limitations. Wherein:

Sakuragi also teaches that: each of the current storage circuits comprises a voltage component holding section, which comprises a capacitance element (C1) in which electric charges corresponding to the operating current are written, which fetches the operating current

outputted from the current generation circuit and holds a voltage component corresponding to a current value of the operating current; wherein the voltage component holding section has a field effect type transistor, e.g., M2, which causes the operating current to flow between a source and a drain thereof, and the capacitance element has at least a parasitic capacitance between the source and a gate of the field effect type transistor, see Fig. 1; wherein each of the current storage circuits comprises a drive current generation section which generates and outputs the drive current having a predetermined current ratio relative to the operating current based on the voltage component held in the voltage component holding section, wherein the drive current generation section comprises a current mirror circuit (M1 and M2) having the predetermined current ratio, wherein the drive current has the same current value at the output terminals, see col. 5, lines 46-54.

Ozawa also teaches that: the display apparatus comprising: a display panel (1) having a plurality of scanning lines (7) arranged in a row direction, a plurality of signal lines (6) arranged in a column direction and the plurality of display pixels (11) which is arranged in the vicinity of an intersection of the respective scanning lines and signal lines and has an optical element; a signal drive circuit (3), the optical element in the display pixel includes a light emitting element, which is an organic electroluminescent element, see Figs. 1-5, and col. 4, lines 46-51.

Official notice is taken for the claimed limitation of: "the mobility of the field effect type transistor has a value which is at least approximately 200 cm.sup.2/Vs or a larger value" because such a value is well known and expected in the art. It would have been obvious to have the gate width (W) and the gate length (L) of each transistor properly designed so that the mobility of the

field effect type transistor is as large as necessary or needed in order to increase mutual conductance for providing high speed and high output switching transistor.

Claims 7-12, 15, 45-49, 60, and 61 are therefore rejected on the same reasons set forth in claim 1, and by the reasons noted above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. They are U.S. Patents Nos.: 6,586,888 ; 6,268,842; and 6,731,273, which teach display systems and methods for supplying drive currents to operate a plurality of light emitting elements arranged in a display panel.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry N. Tran whose telephone number is 571-272-7760. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H. Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Henry N. Tran

Henry N Tran
Primary Examiner
Art Unit 2629

HT
5/11/07